Improvement in Sub-circuit of Full Adder Cell (XOR and XNOR) by GDI and FinFET Structure

Hamed Sadeghi, Hamed Mohammadi Jirandeh, Ali Zakeri

Abstract— Full adders are the basic block of many circuits i.e. CPU and ALU. Full swing for good driving is one of the main features of full adders and its sub circuits (XOR/XNOR). In this paper we propose full swing XOR/XNOR by combining of GDI and FinFET techniques. Our proposed circuit has been compared with the other circuits, In terms of average power, delay, Swing and PDP. Simulation results with FinFET show that the proposed circuit average power is 1.3× greater than the best circuit [3], but offers 1.4× improvement in delay, 1.2× improvement in swing and finally 1.04× improvement in PDP. All Simulations are carried out by HSPICE in TSMC 32nm CMOS technology.

Index Terms— Full Adders, XOR/XNOR, Full swing, GDI, FinFET.

1 Introduction

Addition is obligatory component of arithmetic operation and the foundation of many other frequently used arithmetic operations [1]. Arithmetic operations are widely used in many VLSI applications such as DSP architectures, video and image processing, and microprocessors [2]. Besides, they are core units of many sub-systems of microprocessor, system on chip, network on chip and application specific instruction-set processor. Therefore full adders influence the overall performance of these systems significantly. Improvement of full adder can be achieved by using the best sub-circuits. Since, XOR and XNOR gates are the most used sub-circuits for designing full adder circuit (See Fig.1), so the enhancing features of XOR and XNOR circuits (XXCs) increase the performance of full adder.

Furthermore, XXCs are major component in various circuits especially circuits used for performing arithmetic operations like full adders, compressors, comparators, etc. They also play important roles in designing parity checker and generator circuits. Because of this reasons, if we design XXC with good quality and optimization, it will improve the performance of larger number of circuits. There are several issues related to XXCs. Some of them are good driving ability, delay, power consumption and area. Full swing XXCs are useful for good driving of next chains in complex circuits. Low-delay and low power consumption improve the performance of a system.

Several designs are available in the literature to realize the XOR/XNOR function using different logic styles [3, 4]. In this paper, Section II will dis-cuss briefly about the GDI and FinFET techniques. We consider the best XXC proposed in [3] and introduce the optimization XXC accomplished by GDI and FinFET techniques with extra transistors in Section III. Simulation results are discussed and compared in Section IV. Finally, the conclusion of the paper appears in Section V.

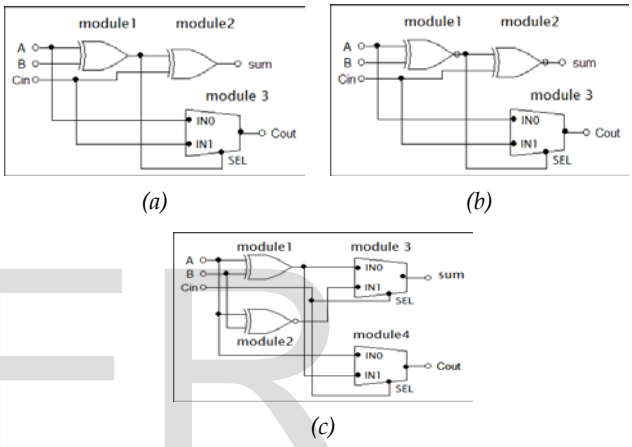

Fig. 1. (a) Group 1: cascaded full adder using two XOR gates; (b) cascaded full adder using two XNOR gates; (c) Centralized full adder [5].

2 State of GDI and FIN-FET Techniques

2.1 Gate-Diffusion Input

The basic Gate-Diffusion Input (GDI) cell is shown in Fig. 2, while the truth table is shown in Table I. At first sight you think, it is an inverter circuit, but with all similarity it is not. Because source of the PMOS in a GDI cell is not connected to VDD, also the source of the NMOS in a GDI cell is not connected to GND.

Hence, we have two extra input pins to use. This feature gives some advantages and also some disa-dvantages. It makes the GDI design more flexible than a usual CMOS design. However the major cause of its disadvantage is special CMOS process required. To be more specific, the GDI scheme requires twin-well CMOS or silicon on insulator (SOI) process to implement, which is of course more expensive than the standard p-well CMOS process[6].

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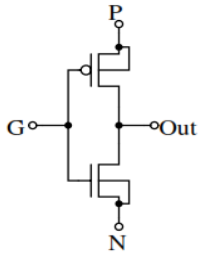

Fig. 2. Basic Gate-Diffusion Input Cell

TABLE I: Truth table of the basic GDI cell

N	P	G	OUT	FUNCTION
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	A+B	0R
B	0	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
0	1	A	$\bar{A}$	NOT

2.2 Fin-type Field-Effect Transistor

Fin-type Field-Effect Transistor (FinFETs) have been proposed as a promising alternative for two fold challenges: (a) minimization of leakage current (subthreshold gate leakage), and (b) reduction in the device-to-device variability to increase yield [7]. Figure 3 illustrates the structure of a multi-fin FinFET. The FinFET device consists of a thin sili-con body, the thickness of which is denoted by Tsi, wrapped by gate electrodes. The current flows para-llel to the wafer plane, whereas the channel is form-ed perpendicular to the plane of the wafer. Due to this reason, the device is termed quasi-planar. The independent control of the front and back gates of the FinFET is achieved by etching away the gate electrode at the top of the channel.

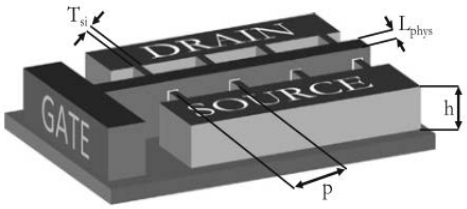

Fig. 3. Multi-fin FinFET

FinFET devices come in many types. As illustrated in Fig. 4(a), in shorted-gate (SG) FinFETs, the two gates are connected together, leading to a three-terminal device.

This can serve as a direct replacement for the conventional bulk-CMOS devices. As demonstrat-ed in Fig.4 (b), in independent-gate (IG) FinFETs, the top part of the gate is etched out, giving way to two independent gates. Because the two independ-ent gates can be controlled separately, IG-mode FinFETs offer more design options [8].

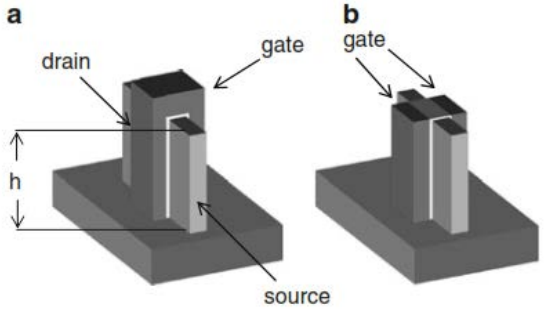

Fig. 4. (a) SG-mode FinFET; (b) IG-mode FinFET

The performance and power characteristics of FinFET logic gates using transistors in various con-nected configurations are explored next. Some gui- delines for "back of the envelope" logic design using FinFETs are also presented. In general, three modes of FinFET logic gates are logically obvious: (1) SG-mode, in which FinFET gates are tied tog-ether; (2) low-power (LP)-mode, in which the back-gate bias is tied to a reverse-bias voltage to reduce subthreshold leakage [9]; and (3) IG-mode, in which independent signals drive the two device gates. A hybrid IG/LP-mode which employs a com-bination of LP and IG modes is also available.

3 Optimization Circuit

Islam et al [3] investigates 15 different XXCS to observe their output levels. This reference, analyzes those XXCs, which propose better output levels in terms of design metrics such as tp (propagation delay) and EDP (energy delay product). It also carries out variability analysis of these parameters. Finally, it translates the best XXC from CMOS into emerging FinFET technology. PTL (pass transistor logic)-based 8-transistor XXC (Fig. 5) is found to be the best in this investigation.

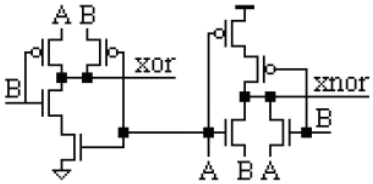

Fig. 5. 8-T XOR/ XNOR circuit in [4]

It offers bad 0 at XOR output for input vector "00", which is clearly observable in simulation waveform shown in Fig. 6. To improvement of the XXCs, we propose new circuit using GDI structure shown in Fig. 7.

Left part of above circuit is GDI XXC [6], [10] which you can see it in Figure 8. As illustrated in truth table of GDI XOR and XNOR (table II), GDI cell-based XXCS have some problems. One of them is bad 1 at XOR for "10" input pattern and another is bad 1 at XNOR for input pattern "11".

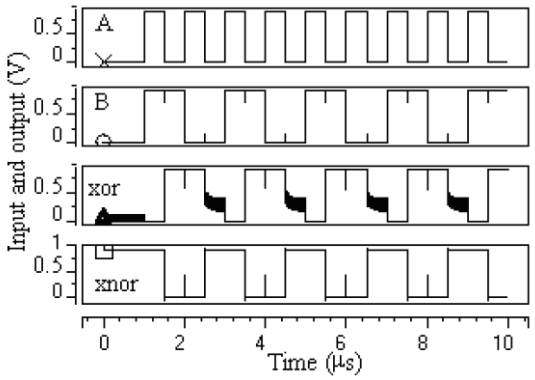

Fig. 6. Monte Carlo simulation [3]

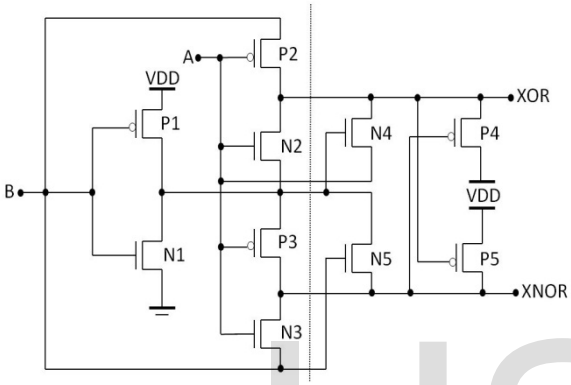

Fig. 7. proposed circuit

TABLE II: Truth table of GDI XOR and XNOR

XOR			XNOR		
A	B	OUT	A	B	OUT
0	0	V_{tp}	0	0	V_{dd}
0	1	V_{dd}	0	1	V_{tp}
1	0	$V_{dd} - V_{tn}$	1	0	0
1	1	0	1	1	$V_{dd} - V_{tn}$

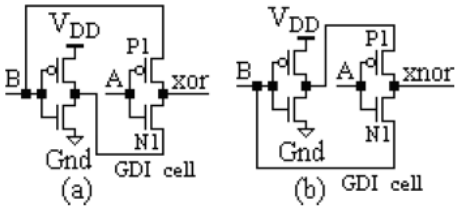

Fig.8: (a) GDI XOR circuit, (b) GDI XNOR circuits [6], [10]

For removing the GDI disadvantages (bad 0 and 1), additional sub-circuit has been proposed, as shown in Fig. 9. This additional sub-circuit adds to right part of Fig. 7. It has four additional transistors. It is proved simply that this circuit can compensate threshold loss. The performance of this part of circuit will look like this, when the input is "00", Output will be V_tp. In case actual output is "0". To solve this problem transistor N4 will pull down the output of XOR to GND. Other transistor (N5, P4, P5) have similar function.

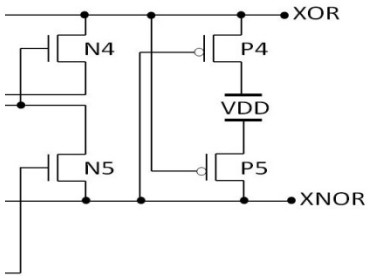

Fig.9: additional sub-circuit

Moreover, delay and average power are decreased clearly by use of FinFET designing with respect to the best XXC (figure 5), as described in next part.

4 SIMULATION RESULTS AND DISCUSSION

In this section, simulation results of the proposed circuit by HSPICE in TSMC 32nm CMOS technol-ogy with 0.9V voltage supply at a frequency of 100 KHz with use of Cout=10fFare presented. Besides, transistors are designed with FinFET structure in SG-mode. The results compare with those came out from [3] (while we tested some of their accuracy). Then, we try to show the improvements in output signals, delay, average power and PDP.

4.1 Output signals

To better compare, output signals of Fig. 5 is shown in Fig. 10. As illustrated in Fig. 10, this circuit has swing problem (problem bad 0 or 1).

As denoted in Fig. 11, output signals of propo-sed circuit have full swing without any threshold loss. So, the problem of bad 0 or 1 is removed. Clearly this full swing circuit brings good driving ability which is obligatory in lots of applications.

4.2 Average power, delay and PDP

Results of table III indicate that, average power of Fig. 7 is more than best XXC (Fig. 5). It is reasonable because the number of transistors is more. While the delay is less. These results are obtained without the FinFET Design.

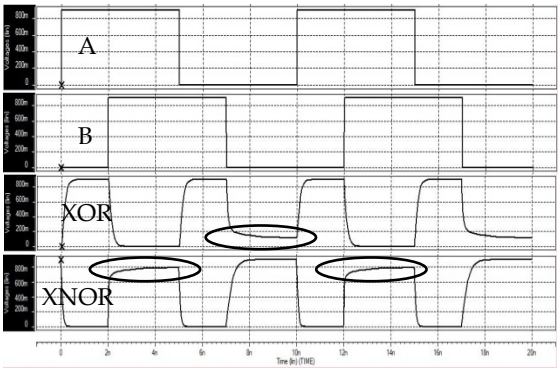

Fig.10: output signal of Fig. 5

FinFET is used to more improvement in delay, power and PDP, which described in Table IV. Although the proposed

circuit has a lot of power consumption, but it has a little delay and generally the PDP of proposed circuit is less than conventional circuit (Fig. 5).

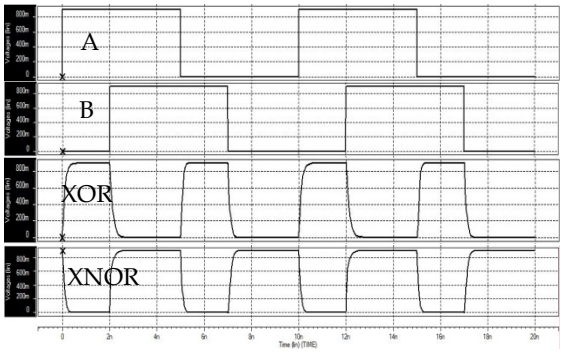

Fig.11: output signal of proposed circuit (Fig. 7)

TABLE III: average power, delay, and swing without FinFET structure

Technology 32n	Ave-power	T-delay	swing
Fig. 5 [3]	3.46e-6	3.03e-10	$V_{dd} - V_t$
Fig. 7 [proposed circuit]	7.43e-6	2.92e-10	V_{dd}

TABLE IV: average power, delay, and swing with FinFET structure

Technology 32n With FINFET	Ave-power	T-delay	swing
Fig. 5 [3]	3.14e-6	9.54e-11	$V_{dd} - V_t$
Fig. 7 [proposed circuit]	4.27e-6	6.77e-11	V_{dd}

TABLE V: PDP with FinFET structure

Technology 32n With FINFET	PDP
Fig. 5 [3]	29.9556
Fig. 7 [proposed circuit]	28.9079

5 Conclusion

This paper presents an XXC utilizes GDI and FinFET techniques. The best improvement of this circuit is being full swing for good driving ability. The importance of this quality appears in complex circuits that XXCs are their sub-circuit.

Simulation results of FinFET with TSMC 32nm show that the proposed circuit average power is 1.3× greater than the best circuit, but offers 1.4× improvement in delay , 1.2× improvement in swing and finally 1.04× improvement in PDP. So by using extra transistors, output signals of proposed circuit have full swing without any threshold loss.

Acknowledgment

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